Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application, where added material is shown in underlined type, deleted material is shown in ~~strikeout type~~:

Listing of Claims:

1-145. (Cancelled)

146. (New) A system for adaptive configuration, the system comprising:

a configurable logic unit including a first plurality of heterogeneous computational elements and a configurable logic interconnection network configurably coupling the first plurality of heterogeneous computational elements, the configurable logic interconnection network adapted to configure the first plurality of heterogeneous computational elements for performing a first logic function in response to first logic configuration information, the configurable logic interconnection network further adapted to reconfigure the first plurality of heterogeneous computational elements for performing a second logic function in response to second logic configuration information, the configurable logic interconnection network including a first memory for storing the first and second logic configuration information; and

a configurable digital signal processing unit including a second plurality of heterogeneous computational elements and a digital signal processing interconnection network coupling the second plurality of heterogeneous computational elements together, the digital signal processing interconnection network adapted to configure the second plurality of heterogeneous computational elements for performing a first digital signal processing function in response to first digital signal processing configuration information, the digital signal processing interconnection network adapted to configure the second plurality of heterogeneous computational elements for performing a second digital signal processing function in response to second digital signal processing configuration information, the digital signal processing interconnection network including a second memory for storing the first and second digital signal processing configuration information.

147. (New) The system of claim 146, wherein the configurable logic interconnection network includes multiplexers that selectively interconnect the first plurality of heterogeneous computational elements for the first logic function in response to the first logic configuration information and

selectively interconnect the second plurality of heterogeneous computational elements for the second logic function in response to the second logic configuration information.

148. (New) The system of claim 147, further comprising a configuration network to selectively route the first and second logic configuration information to the first memory and the first and second digital signal processing configuration information to the second memory.

149. (New) The system of claim 146, wherein the configurable logic interconnection network is adapted to configure at one point in time the first plurality of heterogeneous computational elements for performing the first logic function in response to the first logic configuration information, and the configurable logic interconnection network is further adapted to reconfigure at another point in time the first plurality of heterogeneous computational elements for performing the second logic function in response to the second logic configuration information.

150. (New) The system of claim 149, wherein the configurable logic computation unit is further configured to determine a system configuration capacity prior to utilizing the second logic configuration information to reconfigure for the second logic function.

151. (New) The system of claim 146, wherein the first plurality of heterogeneous computational elements of the configurable logic computational unit includes a first type of heterogeneous computational element for performing a first operation and a second type of heterogeneous computational element for performing a second operation.

152. (New) The system of Claim 151, wherein the first and second types of heterogeneous computational elements are each a different one of an adder, a multiplier, a register, and a function generator.

153. (New) The system of claim 152, wherein the first plurality of heterogeneous computational elements of the configurable logic computational unit further includes a third type of heterogeneous computational element for performing a third operation from the group of an adder, a multiplier, a register, or a function generator having data inputs and a control input to select a specific function.

154. (New) The system of claim 146, wherein the first logic function is a combinational logic function, arithmetic function or a register function, and the second logic function is a combinational logic function, arithmetic function or a register function.

155. (New) The system of claim 146, wherein the second plurality of heterogeneous computational elements of the digital signal processing computational unit each perform a different function from the group of multiplication, addition, subtraction, accumulation, summation and dynamic shift.

156. (New) The system of claim 146, wherein the second memory is also for storing a third digital signal processing configuration information, and wherein the digital signal processing interconnection network is adapted to configure its second plurality of heterogeneous computational elements to perform another digital signal processing function in response to the third digital signal processing configuration information.

157. (New) The system of claim 156, wherein the other digital signal processing function is one of fixed point arithmetic function, floating point arithmetic functions, filters, and transformation functions.

158. (New) The system of claim 146, wherein at least one of the respective logic and digital signal processing configuration information is transferred to the system from a machine-readable medium.

159. (New) The system of claim 146, wherein the respective logic and digital signal processing configuration information are each transmitted to the system through a wireless interface.

160. (New) The system of claim 146, wherein the respective logic and digital signal processing configuration information are each embodied as a plurality of discrete information data packets.

161. (New) The system of claim 146, wherein the respective logic and digital signal processing configuration information are each embodied as a stream of information data bits.

162. (New) The system of claim 146, wherein the configurable logic computation unit is further configured to generate a request for another logic configuration information to reconfigure the first plurality of heterogeneous computational elements to perform another logic function.

163. (New) The system of claim 146, wherein the configurable logic computation unit is further configured to determine a system configuration capacity prior to utilizing the other logic configuration information to reconfigure for the other logic function.

164. (New) The system of claim 146, wherein the digital signal processing unit is further configured to determine a system configuration capacity prior to utilizing the second digital signal processing configuration information to configure for the second digital signal processing function.

165. (New) The system of claim 146, wherein the second plurality of heterogeneous computational elements of the digital signal processing computational unit includes a multiplier computational element and an adder computational element.

166. (New) The system of claim 146, wherein the first plurality of heterogeneous computational elements is different than the second plurality of heterogeneous computational elements.

167. (New) A system for adaptive configuration, the system comprising:

a configurable logic unit including a first plurality of heterogeneous computational elements and a configurable logic interconnection network configurably coupling the first plurality of heterogeneous computational elements together, the configurable logic interconnection network adapted to configure the first plurality of heterogeneous computational elements for performing a plurality of logic functions in response to respective sets of logic configuration information, the configurable logic interconnection network including a first memory for storing the respective sets of logic configuration information; and

a configurable digital signal processing unit including a second plurality of heterogeneous computational elements and a digital signal processing interconnection network coupling the second plurality of heterogeneous computational elements, the second plurality of heterogeneous computational elements including a multiplier computational element and an adder computational element, the digital signal processing interconnection network adapted to configure the second plurality of heterogeneous computational elements for performing a plurality of digital signal processing functions in response to respective sets of digital signal processing configuration information, the digital signal processing interconnection network including a second memory for storing the respective sets of digital signal processing configuration information.

168. (New) The system of claim 167, wherein the first plurality of heterogeneous computational elements of the configurable logic computation unit may include an adder, a register, or a function generator having data inputs and a control input to select a specific function.

169. (New) The system of claim 167, wherein the digital signal processing interconnection network includes multiplexers coupled to the multiplier and adder computational elements, the multiplexers routing data between the multiplier and adder computational elements.

170. (New) The system of claim 167, wherein the digital signal processing interconnection network provides another configuration information to configure the digital signal processing computational unit to perform another function.

171. (New) The system of claim 170, wherein the other function is one of fixed point arithmetic function, floating point arithmetic functions, filters, and transformation functions.

172. (New) The system of claim 167, wherein the heterogeneous computational elements of the digital signal processing computational unit each perform a function from the group of subtraction, accumulation, summation and dynamic shift.

173. (New) The system of claim 167, wherein the first plurality of heterogeneous computational elements is different than the second plurality of heterogeneous computational elements.

174. (New) A system for adaptive configuration, the system comprising:

a configurable logic unit including a first plurality of heterogeneous computational elements and a configurable logic interconnection network configurably coupling the first plurality of heterogeneous computational elements, the configurable logic interconnection network adapted to configure the first plurality of heterogeneous computational elements for performing a first logic function in response to first logic configuration information, the configurable logic interconnection network adapted to configure the first plurality of heterogeneous computational elements for performing a second logic function in response to second logic configuration information; and

a configurable digital signal processing unit including a second plurality of heterogeneous computational elements and a digital signal processing interconnection network configurably coupling the second plurality of heterogeneous computational elements, the second plurality of heterogeneous elements including a first type of computational element and a second type of computational element, the digital signal processing interconnection network adapted to configure the second plurality of heterogeneous computational elements for performing a first digital signal processing function in response to first digital signal processing configuration information by bypassing the first type of computational element, the digital signal processing interconnection network adapted to configure the second plurality of heterogeneous computational elements for performing a second digital signal processing function in response to second digital signal processing configuration information by connecting the first and second types of computational elements, the digital signal processing interconnection network includes a memory for storing the first and second digital signal processing configuration information.

175. (New) The system of claim 174, wherein the heterogeneous computational elements of the configurable logic computational unit are each one of a group of an adder, a multiplier, a register, or a function generator having data inputs and a control input to select a specific function.

176. (New) The system of claim 174, wherein the digital signal processing interconnection network includes multiplexers coupled to the two types of computational elements, the multiplexers routing data between the two types of computational elements.

177. (New) The system of claim 174, wherein the heterogeneous computational elements of the digital signal processing computational unit each perform a function from the group of multiplication, addition, subtraction, accumulation, summation and dynamic shift.

178. (New) The system of claim 146, wherein the respective configuration information are each received by the system and stored in the respective memory.

179. (New) The system of claim 146, wherein the received respective configuration information are each encrypted.

180. (New) The system of claim 146, wherein the received respective configuration information were each transmitted to the system in response to a request sent by the system.

181. (New) The system of claim 174, wherein the first plurality of heterogeneous computational elements is different than the second plurality of heterogeneous computational elements.